Lab 14 Part 3
Output Compare, Port A

1. Assemble the circuit shown in Fig. 1

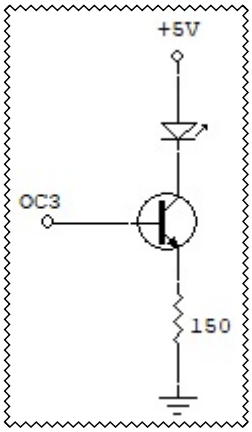

Fig. 1

2. Create, assemble make appropriate comments and save the following program:

```
        ORG     $0100
        LDAA    #$03            ;PRESCALER, SLOW DOWN E-CLOCK (03=slowest)
        STAA    $1024           ;timer interrupt mask 2 (prescaler)

        LDAA    #$54            ;toggle  PIN 28, 29 AND 30
        STAA    $1020           ;
        LDY     #$1000          ;store pattern in TCTL1

        CLR     $1018           ;clear TOC2, memory location to hold time calculations
        CLR     $1019
        CLR     $101A           ;clear TOC3, memory location to hold time calculations
        CLR     $101B
        CLR     $101C           ;clear TOC4, memory location to hold time calculations
        CLR     $101D

*Start the process              ;TFL1 $1023
LOOP    NOP                     ;enable OC2,OC3,OC4
        BSET    $23,Y,#$70      ;

WAITFLG         BRCLR           $23,Y,#$70 WAITFLG   ;wait flag clear, output compare completed

        LDD     $1018           ;slowest speed
        LDD     $1019
        ADDD    #$FFFF
        STD     $1018           ;output compare 2
        STD     $1019

        LDD     $101A           ;faster speed
        LDD     $101B
        ADDD    #$7FFF
        STD     $101A
        STD     $101B           ;output compare 3

        LDD     $101C           ;fastest speed
        LDD     $101D
        ADDD    #$3FFF
        STD     $101C           ;output compare 4
        STD     $101D

        BRA     LOOP
        END
```

3. The original program should produce a square wave at Output Compare 2, 3,4; Pin 28, 29, 30
*List of registers

```
*TOC2           $1018   Timer Output Compare 2*
*TOC3           $101A   Timer Output Compare 3*
*TOC4           $101C   Timer Output Compare 4*
*TCTL1          $1020   Timer Control1*
*TMSK1          $1022   Timer Interrupt Mask 1*
*TFLG1          $1023   Timer Interrupt Flag 1*
*TMSK2          $1024   Timer Interrupt Flag 2*
```

*Commands :	LDD	Load Double Accumulator
	ADDD	Add to double accumulator
	STD	Store double accumulator
	BRA	Branch always
	BSET	Bit set
	BRCLR	Branch if clear